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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/704,156	11/01/2000	Takeshi Wakabayashi	00791/LH	3188

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EXAMINER	
THAI, LUAN C	

ART UNIT	PAPER NUMBER
2827	#6

DATE MAILED: 02/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/704,156	Applicant(s) WAKABAYASHI, TAKESHI
	Examiner Luan Thai	Art Unit 2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *1-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II, claims 11-16, in Paper No. 5 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 11-12 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshikazu (5,989,982 applicant's admitted prior art).

Regarding claims 11-12, Yoshikazu teaches (figures 1-6, especially see figures 2A-2H) a method manufacturing a semiconductor device comprising the steps of: preparing a semiconductor wafer 5 having an upper surface, a lower surface opposing the upper surface, sides extending between the upper and lower surfaces, a plurality of outer connection terminals 2 formed on the upper surface; adhering a dicing tape 7 to the semiconductor wafer; making trenches (figures 2b-2c) in those parts of the wafer which lie between chip-forming regions thereof, each trench extending through the thickness of the wafer from the upper surface; forming a seal film 12 on the upper surface of the wafer, filling the

trenches and exposing the outer connection terminal 2 at one surface; cutting the seal film 12 along the trenches (figures 2g-2h), removing those parts of the seal film which have a smaller width than the trenches; peeling the dicing tape 7 from the semiconductor wafer.

Regarding claim 15, Yoshikazu teaches (figures 1-6, especially see figures 2A-2H) a method manufacturing a semiconductor device comprising the steps of: preparing a semiconductor wafer 5 having an upper surface, a lower surface opposing the upper surface, sides extending between the upper and lower surfaces, a plurality of outer connection terminals 2 formed on the upper surface; adhering a seal film 7 on a lower surface of the semiconductor wafer; making trenches (figures 2b-2c) in those parts of the wafer which lie between chip-forming regions thereof, each trench extending through the thickness of the wafer from the upper surface; forming another seal film 12 on the upper surface of the wafer, filling the trenches and exposing the outer connection terminal 2 at one surface; cutting the seal film 12 along the trenches (figures 2g-2h), removing those parts of the seal film which have a smaller width than the trenches.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikazu (5,989,982 applicant's admitted prior art) in view of Sasaki et al. (5,888,883).

Regarding claims 13 and 14, Yoshikazu discloses all the steps of the claimed invention as detailed above except for the step of adhering a support tape to an upper surface of the seal film after the seal film being cut (as recited in claim 13), and a step of polishing a lower surface of the semiconductor wafer.

Sasaki et al. teach (Figures 8-23, especially see figures 8-10) a method for making a semiconductor device including a step of adhering a support tape 26 to an upper surface of the seal film after the seal film being cut in order to process the next step of polishing the lower surface of the semiconductor wafer, thereby reducing the thickness of the semiconductor wafer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Sasaki et al.'s teachings to Yoshikazu process in order to effectively perform the step of polishing the lower surface of the semiconductor wafer, thereby reducing the thickness of the semiconductor wafer.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (6,159,837) in combination with Yoshikazu (5,989,982 applicant's admitted prior art).

Regarding claim 16, Yamaji et al. teach (1-6, Col. 2) a method of making a semiconductor device comprising the steps of: preparing a semiconductor wafer 1 having an upper surface and sides and having a plurality of connection pads 2

on the upper surface; forming an insulating 3 having openings exposing the connection pads 2, thereby covering the upper surface of the wafer; forming wirings 4 on the insulating film 3, the wirings connected to the connection pads 2; forming pillar-shaped electrodes 7 on the wirings; forming a seal film 5 exposing the pillar-shaped electrodes 7 at one surface (e.g., top surface) and covering the upper surface of the semiconductor wafer. Yamaji et al. fail to teach that the seal film 5 also cover the sides of the semiconductor wafer.

Yoshikazu while related to a similar method of making a semiconductor device teach (figures 1-6, especially see figures 2A-2H) the seal film 12 not only covering the upper surface of the semiconductor wafer 1 but also covering the side surfaces of the semiconductor wafer in order to obtain high resistance to the peeling of the resin applied to the sides (Col. 3, lines 19+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Yoshikazu teachings to Yamaji et al.'s method in order to obtain high resistance to the peeling of the resin applied to the sides of the semiconductor wafer.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is (703) 308-1211. The examiner can normally be reached on 7:00 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Talbott can be reached on (703) 305-9883. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Luan Thai
February 1, 2002

DAVID L. TALBOTT
PRIMARY EXAMINER
ART UNIT 2827